Remarks

Reconsideration of this application is respectfully requested.

Claims 1-15 are pending in the application, with claims 1, 6, 8, 11, and 14 being the independent claims.

Based on the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Reconsideration of this Application is respectfully requested.

Applicants note the Examiner's remarks with respect to the terms "clock credit," "test bench," and "clock arbitrator" (Office Action, p. 2). Applicants submit that each of these terms has a clear plain meaning and is properly interpreted as being broad enough to include, but not be limited to, the examples provided throughout the specification and the example interpretation provided by the Examiner. While the Applicants do not acquiesce in the Examiner's interpretation, even if the Examiner's interpretation is accepted for the sake of argument, the Applicants contend that the invention is nonetheless patentable.

Rejections under 35 U.S.C. § 103

Claims 1-5 and 11-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent 5,732,247 ("Dearth '247") in view of U.S. patent 5,790,829 ("Flynn"), and in further view of U.S. patent 5,363,319 ("Okuda") and in further view of the Microsoft Press Computer Dictionary, 3d Edition ("Microsoft") (Office Action, p. 3, sect. 4). Applicants respectfully traverse.

These four references are not all applied by the Examiner to each of these rejected claims. Rather, these references are combined in different ways to particular claims.

With respect to claim 1, the Examiner argues that this claim is rendered obvious by a combination of Dearth '247 and Flynn. The Examiner argues that while Dearth '247 does not disclose issuing a clock credit or token to control simulation modules, Flynn discloses the use of a token to control module execution (Office action, pp3, 4).

As stated on page 6 of the specification for the present invention, a clock credit is a token issued to a simulation module and having a numerical value, permitting a device under test (DUT) to execute for some number of clock cycles associated with the value of the clock credit. Execution stops after the clock cycles have been used. Neither Flynn nor Dearth '247 discloses such a clock credit. While Flynn discloses "tag event structures" that mark the conclusion of processing of a family of "event structures," these tag event structures do not represent clock credits. Rather, tag event structures, according to Flynn, mark the completion of processing of previously-sent event structures (Flynn, column 9, lines 23-31). The tag event structures are used to mark checkpoints for synchronization purposes (Flynn, column 3, line 62- column 4, line 2). There is no disclosure in Flynn (or Dearth '247) of a tag or token that has a value associated with a number of clock cycles for which a simulation module is to execute. The issuance of a clock credit, as the term is used in the present application, is therefore absent from Dearth '247 and Flynn. The combination of these two references therefore fails to render claim 1 obvious. Moreover, claims 2-5 depend from claim 1 and necessarily incorporate all the limitations described in claim 1. Claims 2-5 are therefore patentable for at least the same reason as claim 1 and further in view of their own

respective features. For at least this reason, none of claims 1-5 are obvious in view of the cited art, taken alone or in combination.

We note that the Examiner has rejected claim 3 as obvious in view of Dearth '247 and Flynn, and further in view of Okuda (Office Action, pp. 4, 5). Okuda, however, fails to overcome the shortcomings of Dearth '247 and Flynn with respect to the clock credit issuance limitation of claim 1. For at least this reason, claim 3 is not obvious in view of the cited art, taken alone or in combination.

The Examiner has also rejected claims 4 and 5 as obvious in view of Dearth '247 and Flynn, and further in view of Microsoft (Office Action, p.5). Microsoft, however, fails to overcome the shortcomings of Dearth '247 and Flynn with respect to the clock credit issuance limitation of claim 1. For at least this reason, neither of claims 4 and 5 is obvious in view of the cited art, taken alone or in combination.

Claim 11 is a computer program product claim that recites computer readable program code logic for causing a computer to execute the steps of method claim 1. The Examiner argues that claim 11 is rendered obvious by a combination of the Dearth '247 and Flynn references. As discussed above, however, the issuance of a clock credit to a simulation module is not disclosed by either Dearth '247 or Flynn, taken alone or in combination. Likewise, computer readable program code logic for causing a computer to issue a clock credit is not disclosed. For at least this reason, therefore, claim 11 is not rendered obvious by a combination of Dearth '247 and Flynn. Moreover, claims 12 and 13 depend from independent claim 11 and necessarily incorporate the limitations specified in claim 11. The limitation of computer readable program code logic for causing a computer to issue a clock credit is therefore present in claims 12 and 13, but

not disclosed by either Dearth '247 or Flynn. For at least this reason, therefore, claims 12 and 13 are not obvious over the art cited by the Examiner.

The Examiner has rejected claim 13 as obvious in view of Dearth '247 and Flynn, and further in view of Okuda (Office Action, pp. 4, 5). Okuda, however, fails to overcome the shortcomings of Dearth '247 and Flynn with respect to the clock credit issuance limitation of claim 11. For at least this reason, claim 13 is not obvious in view of the cited art, taken alone or in combination.

Claims 6, 7, 14, and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patents 5,905,883 ("Kasuya") and 5,081,601 ("Eirikasson") and further in view of Microsoft.

With respect to claim 6, the Examiner argues that this claim is rendered obvious by a combination of Kasuya and Eirikasson. In particular, the Examiner argues that Kasuya discloses the steps of reading the specification information, identifying a device under test, and determining the interface to the DUT (Office Action, pp. 5, 6). Kasuya, however, does not disclose these steps. Kasuya discloses a test bench that performs stimulus generation and output comparisons (Kasuya, col. 2, lines 1, 2), but never discusses steps for creating a test bench, apart from creation and compilation of a test bench source file (Kasuya, col. 4, line 66 through col. 5, line 2). Eirikasson likewise fails to disclose these steps. Eirikasson discloses interconnection and coordination of simulators (Eirikasson, col. 4, lines 13-29), but never addresses steps for creating a test bench. Kasuya and Eirikasson, either alone or in combination, therefore fails to render claim 6 obvious. Claim 7 depends from independent claim 6, and necessarily includes

all the limitations of claim 6. Because a combination of Kasuya and Eirikasson fails to disclose all the limitations of claim 6, it likewise fails to disclose all the limitations of claim 7. Claim 7 is therefore not obvious in view of the cited art.

Claim 14 is a computer program product claim that recites computer readable program code logic for causing a computer to perform the steps of claim 6. While the Examiner argues that a combination of Kasuya and Eirikasson renders claim 14 obvious (Office Action, p. 6), this combination fails to disclose the limitations pertaining to identification of a DUT, determination of an interface to a DUT, and generation of a test bench component for the DUT. Kasuya discloses a test bench that performs stimulus generation and output comparisons (Kasuya, col. 2, lines 1, 2), but never discusses program code logic for creating a test bench, apart from creation and compilation of a test bench source file (Kasuya, col. 4, line 66 through col. 5, line 2). Eirikasson likewise fails to disclose program code logic for these steps. Eirikasson discloses interconnection and coordination of simulators (Eirikasson, col. 4, lines 13-29), but never addresses program code logic for creating a test bench. Kasuya and Eirikasson, either alone or in combination, therefore fails to render claim 14 obvious.

With respect to claim 14, the Examiner also states that Microsoft discloses computer readable code that is executed from a computer readable medium (Office Action, pp. 6, 7). This reference, however, fails to overcome the shortcomings of Kasuya and Eirikasson with respect to program code logic that identifies a DUT, determines an interface to a DUT, and generates a test bench component. Kasuya, Eirikasson, and Microsoft, either alone or in combination, therefore fail to render claim 14 obvious.

Because claim 15 depends from claim 14 and incorporates all the limitations of claim 14, claim 15 is likewise is not rendered obvious by this combination of references.

The Examiner has rejected claims 8-10 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,115,823 ("Velasco") in view of U.S. Patent 5,848,236 ("Dearth '236") and further in view of the article "VHDL for Programmable Logic" ("Skahill") and further in view of U.S. Patent 5,603,015 ("Kurosawa") (Office Action, p. 7).

In particular, the Examiner rejects claim 8 as being unpatentable over a combination of Velasco, Dearth '236, and Skahill. The Examiner argues that Velasco discloses the use of a clock arbitrator (Office Action, pp. 7, 8). Velasco, however, fails to disclose a clock arbitrator wherein a programming language interface (PLI) receives a clock credit from the clock arbitrator. Moreover, while the Examiner argues that Skahill teaches a PLI, Skahill fails to teach a PLI that receives a clock credit from a clock arbitrator. Likewise, Dearth '236 fails to disclose these limitations. For at least these reasons, therefore, the combination of Dearth '236, Skahill, and Velasco fails to render claim 8 obvious. Because claims 9 and 10 depend from independent claim 8, claims 9 and 10 necessarily include all the limitations of claim 8. Because the cited art fails to disclose a clock arbitrator and a PLI that receives a clock credit from the clock arbitrator, the above combination of references fails to render claims 9 and 10 obvious.

With regard to claim 9, the Examiner also argues that Kurosawa discloses a shared memory interface (Office Action, p. 8). Kurosawa, however, fails to compensate for the shortcomings of Dearth '236, Skahill, and Velasco with respect to the limitations of a clock arbitrator and a PLI, wherein the PLI receives a clock credit from the clock

arbitrator. Hence claim 9 is not obvious in view of Dearth '236, Skahill, Velasco, Kurosawa, or any combination thereof.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Edward W. Yee
Attorney for Applicant
Registration No. 47,294

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1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600